Amendments to the Specification

Please amend the Title as follows:

A1

DATA RECORDING CLOCK SIGNAL GENERATOR <u>FOR GENERATING A RECORDING CLOCK SIGNAL FOR RECORDING DATA ON A RECORDABLE MEDIUM</u>

On page 6, please amend the paragraph spanning lines 2-10 as follows:

A2

In the conventional recording clock generating circuit, the phase of the recording clock signal WCLK is constantly synchronous with the wobble signal WBL, as long as the wobble signal is properly detected. However, minor defects might exist on the optical disk, or dirt or dust ~~night~~ <u>might</u> stick to the surface of the optical disk. At the locations corresponding to those defects or the areas to which dirt or dust sticks, the wobble signal is lost, and cannot be detected properly.

On page 21, please amend the paragraph spanning lines 1-4 as follows:

A3

A full-count output (=15) of the counter A 451, which is a signal indicating that the maximum value of the count value of the counter A 451 is "15", is inputted into an input [[L]] <u>S</u> of the synchronous SRFF 455.

On page 21, please amend the paragraph spanning lines 5-8 as follows:

A4

A full-count output (=7) of the counter B 452, which is a signal indicating that the maximum value of the count value of the counter B 452 is "7", is inputted into an ~~output~~ <u>input</u> R of the synchronous SRFF 455.

On page 21, please amend the paragraph spanning lines 14-18 as follows:

A5

A value selected from values "7", "8", and "9" by the multiplexer 454 is inputted into a data input Di of the counter A 451. When the load input LD becomes active (i.e., the ~~lead~~ load input LD is "1"), the count value of the counter A 451 is set at "7", "8", or "9".

On page 23, please amend the paragraph spanning lines 7-14 as follows:

A6

The divided clock counter 46 inputs 2-bit count data from the divided clock counter 46 and 2-bit data as the frequency dividing condition setting value are inputted ~~and 2-bit data as the frequency dividing condition setting value~~ into the frequency dividing rate setting table 47. The frequency dividing rate setting table 47 outputs a frequency dividing rate control signal in accordance with a truth table shown in Table 1, based on the count value of the divided clock counter 46 and the frequency dividing condition setting value ~~of the divided clock counter 46~~.

On page 30, please amend the paragraph spanning lines 7-14 as follows:

A7

The operating time constant of the PLL circuit is generally a cycle longer than a phase comparison cycle. Even if the phase of the divided clock is varied as above, the frequency of the recording clock signal is maintained at a substantially ~~contact~~ constant value, thereby achieving a locked state in which the average phase of the divided clock signal coincides with the phase of the wobble signal in the steady state.

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